RESILIENT Computing

RadPC

SINGLE-BOARD COMPUTER (RADPC-SBC-001)

OVERVIEW

The RadPC Single-Board Computer (SBC) provides radiation-tolerant computing for small spacecraft missions. The RadPC SBC implements quad-redundant computing cores on a commercial Field Programmable Gate Array (FPGA) and deploys a series of patented recovery algorithms to automatically detect, recover, and repair faults caused by single event effects (SEEs). The recovery procedures are abstracted from the user allowing the developer to treat the RadPC SBC as a traditional embedded computer without worrying about SEEs. RadPC uses the popular 32-bit RISC-V CPU, which allows developers to take advantage of open source development tools and libraries.

The RadPC-SBC-001 version is optimized for small spacecraft applications by providing low power consumption and increased computation relative to other commercially available SmallSat computers. The RadPC computer is implemented on an industrial grade Xilinx Artix-7 200T FPGA with an operating temperature of -40C to +100C. This commercial off-the-shelf FPGA is fabricated using a 28nm process node. This reduced feature size provides inherent immunity to total ionizing dose (TID) with a predicated rating exceeding 100krad. Reliability models show the RadPC architecture implemented on an Artix-7 FPGA provides a significant improvement to the Mean Time Before Failure (MTBF) over a simplex system, a system using triple modular redundancy (TMR), and a system using TMR+repair.

FEATURES

- 32-Bit Integer RISC-V CPU (RV32I)
- 12k Data + 12k Instruction On-Chip Memory
- 4M Off-Chip Non-Volatile Storage
- 32 MIPs of Computational Performance
- +5 VDC Single-Input Power Supply
- <2 W Total System Power Consumption
- 100mm x 100mm CubeSat form factor
- PC/104+ Compatible
- 64 Bidirectional, General-Purpose I/O Ports
- 2x UART, 1x SPI, 1x I2C Serial Peripherals
- On-Board MSP430 Housekeeping MCU
- Local Power Regulation with Voltage/Current Monitors
- LEO Reliability: 1556% improvement of MTBF beyond a simplex system and 331% improvement beyond TMR
- Lunar Reliability: 337% improvement of MTBF beyond a simplex system and 67% improvement beyond TMR
- Support for future hardware accelerator coprocessor upgrades

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This document replaces all prior versions for RadPC-SBC-001

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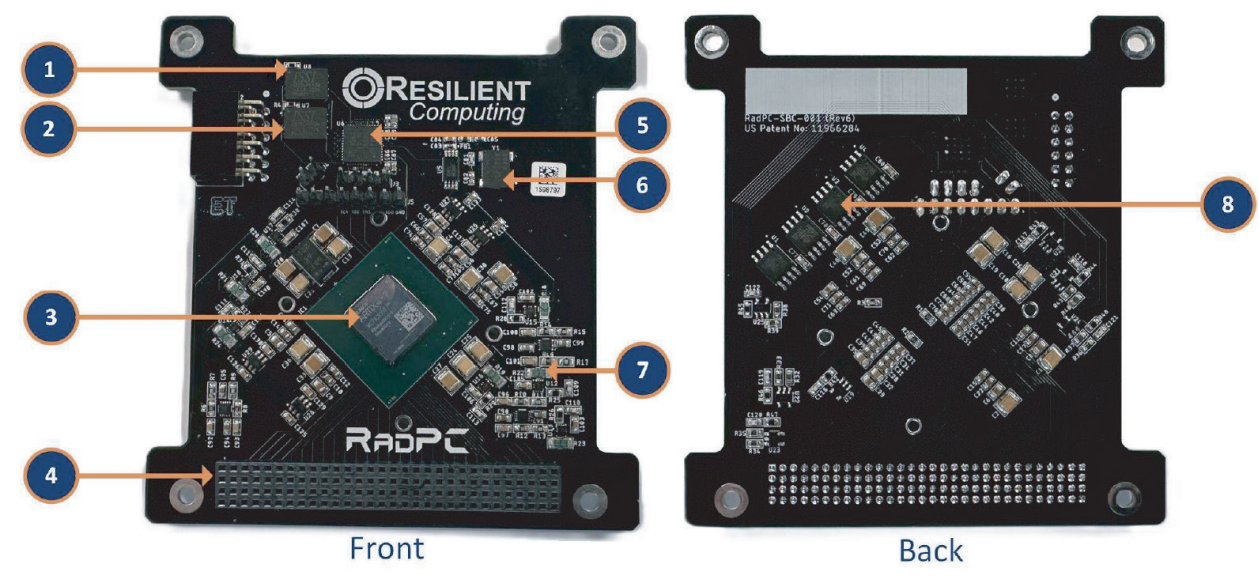
SBC HARDWARE OVERVIEW



1

Non-volatile Bitstream Storage

2

Non-volatile State-of-Health Storage

3

AMD Artix-7 200T FPGA Running RadPC

4

120-Pin, PC/104+ Compatible Connector

5

16 MHz On-Board Oscillator

6

TI MSP430 Housekeeping MCU (MSP430FR5969-SP Rad-Hard Option Available)

7

Local Power Regulation with Voltage/Current Monitors

8

Quad-Redundant Non-Volatile Memory

DEVELOPMENT ENVIRONMENT

Software is developed using the open source RISC-V tools with a custom RadPC plug-in. This allows software to be written in a widely popular development environment with a growing number of open source libraries and tools. Implementation on the RadPC architecture is abstracted from the developer so the system is treated as any standard embedded flight computer.

FLIGHT HERITAGE

RadPC has been developed under NASA funding over the past decade. The RadPC fault tolerant computing architecture has been tested on high altitude balloons (8x), sounding rockets (2x), on the International Space Station (3x), and on small satellites (2x). In 2024, RadPC will be tested on the surface of the moon through NASA's Commercial Lander Services (CLPS) program.

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